On One-Multiplier Implementations of FIR Lattice Structures

ZINNUR DOĞANATA AND P. P. VAIDYANATHAN

Abstract — **One-multiplier realizations for certain recently reported FIR lossless lattice structures are investigated. The multiplier extraction approach is used to show that there does not exist a real one-multiplier realization whereas it is possible to get complex one-multiplier realizations. This is unlike the situation in conventional linear-prediction FIR lattice structures, where real one-multiplier realizations are possible.**

I. Introduction

Recently a procedure has been outlined for the synthesis of a cascaded lossless lattice structure that can realize any pair of power-complementary FIR transfer functions [1]. Each building block of the structure has four multipliers. However it is possible to obtain a denormalized structure which has only two multipliers per building block from the previous one, by proper scaling. The denormalized structure is shown in Fig. 1. Since it resembles the LPC lattice which has one-multiplier realizations, it is natural to ask if we can reduce the number of multipliers per building block to one. In this correspondence we use the *multiplier extraction approach* [2] to show that it is not possible to get structures that have one real multiplier per building block. This is unlike the situation in conventional linear-prediction FIR lattice structures, where real one-multiplier realizations are possible. The multiplier extraction approach also places in evidence a second derivation of the one-multiplier structure derived in [3], for the well-known FIR lattice [4].

II. One-Multiplier Realizations for the Cascaded Lossless Lattice

The denormalized structure of Fig. 1 is a cascade of building blocks separated by delays. The input–output equations corresponding to a building block are given by

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \boldsymbol{S}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = s\begin{pmatrix} 1 & -\alpha \\ \alpha & 1 \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} \quad (1)$$

where s is a nonzero but otherwise arbitrary scale factor. We wish to find a new building block that will realize (1) with only one multiplier m. We, therefore, consider the constrained three-pair [5] shown in Fig. 2, that contains only adders and multiplierless connections. The input–output equations of the three-pair are given in matrix form as

$$\begin{pmatrix} y_1 \\ y_2 \\ y_3 \end{pmatrix} = \boldsymbol{T}\begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} = \begin{pmatrix} t_{11} & t_{12} & t_{13} \\ t_{21} & t_{22} & t_{23} \\ t_{31} & t_{32} & t_{33} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} \quad (2)$$

where t_{ij} are the transfer parameters. Constraining t_{33} to be zero

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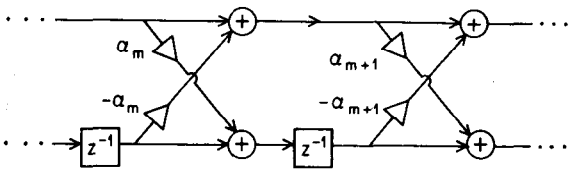

Fig. 1. The denormalized lattice structure.

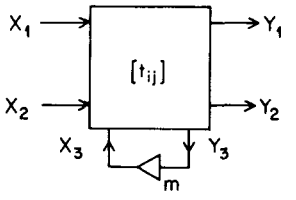

Fig. 2. The constrained three-pair.

in order to avoid a delay-free loop, we have

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \begin{pmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} t_{13} \\ t_{23} \end{pmatrix} x_3 \quad (3a)$$

$$y_3 = \begin{pmatrix} t_{31} & t_{32} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} \quad (3b)$$

$$x_3 = m y_3 = m\begin{pmatrix} t_{31} & t_{32} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix}. \quad (3c)$$

Substituting (3c) in (3a), we get

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \begin{pmatrix} t_{11} + m t_{13} t_{31} & t_{12} + m t_{13} t_{32} \\ t_{21} + m t_{23} t_{31} & t_{22} + m t_{23} t_{32} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix}. \quad (4)$$

Comparing (4) with (1), we conclude that a one-multiplier realization must necessarily satisfy

$$t_{11} + m t_{13} t_{31} = s \quad (5a)$$

$$t_{12} + m t_{13} t_{32} = -s\alpha \quad (5b)$$

$$t_{21} + m t_{23} t_{31} = s\alpha \quad (5c)$$

$$t_{22} + m t_{23} t_{32} = s. \quad (5d)$$

If there exist m and s such that (5a) to (5d) hold for an arbitrary real-valued α and a fixed matrix $\boldsymbol{T} = [t_{ij}]$ independent of both m and α, the following equations must hold:

$$t_{11} = t_{22} \quad (6a)$$

$$t_{13} t_{31} = t_{23} t_{32} \quad (6b)$$

$$t_{12} = -t_{21} \quad (6c)$$

$$t_{13} t_{32} = -t_{23} t_{31}. \quad (6d)$$

Using (6b) and (6d) we can write

$$t_{31}^2 + t_{32}^2 = 0. \quad (7)$$

If we restrict t_{ij} to be real, (7) implies that t_{31} and t_{32} are both zero and thus (5a) to (5d) become

$$t_{11} = s \quad t_{12} = -s\alpha \quad t_{21} = s\alpha \quad t_{22} = s \quad (8)$$

which implies that $t_{11}/t_{12} = -1/\alpha$. Therefore, there does not exist a real one-multiplier realization for the cascaded lossless lattice.

If we permit t_{ij} to be complex, then (6a)–(6d) can be satisfied. For example, we can choose $t_{13} = t_{32} = 1$, $t_{23} = t_{31} = j$ to satisfy

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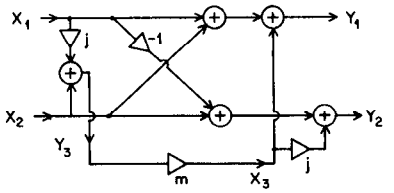

Fig. 3. A complex one-multiplier realization.

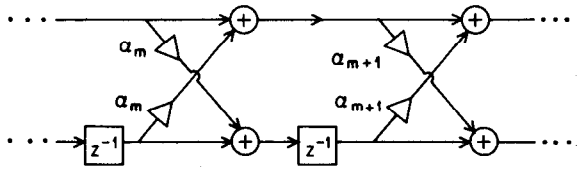

Fig. 4. The LPC lattice.

(6b),(6d) and choose $t_{11}=t_{12}=-t_{21}=t_{22}=1$ to satisfy (6a), (6c). With this choice of $\boldsymbol{T}=[t_{ij}]$, we have

$$s=1+jm, \quad \alpha=-(1+m)/(1+jm) \tag{9}$$

or equivalently, in terms of α

$$s=(1-j)/(1+j\alpha) \quad m=-(1+\alpha)/(1+j\alpha). \tag{10}$$

The resulting structure is shown in Fig. 3.

III. One-Multiplier Realizations for the FIR LPC Lattice

A well-known FIR lattice structure is the one that arises in the context of linear predictive coding [4]. As shown in Fig. 4, this structure has two multipliers in each building block. The input–output equations corresponding to a building block are given as

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \boldsymbol{S}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = s\begin{pmatrix} 1 & \alpha \\ \alpha & 1 \end{pmatrix}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix}. \tag{11}$$

It is known that other lattice forms can be derived based on this one. Makhoul [3] has derived some intermediate lattice structures from which he obtains one-multiplier structures that realize (11). In the following, the same one-multiplier realization is derived directly using the multiplier extraction approach.

Comparing (4) and (11), we write

$$\begin{aligned} t_{11}+mt_{13}t_{31}&=s \quad & t_{12}+mt_{13}t_{32}&=s\alpha \\ t_{21}+mt_{23}t_{31}&=s\alpha \quad & t_{22}+mt_{23}t_{32}&=s. \end{aligned} \tag{12}$$

If we choose

$$t_{22}=t_{11}=1 \quad t_{12}=t_{21}=0 \tag{13}$$

equation (12) becomes

$$1+mt_{13}t_{31}=s \quad mt_{13}t_{32}=s\alpha \quad mt_{23}t_{31}=s\alpha \quad 1+mt_{23}t_{32}=s. \tag{14}$$

With $t_{13}=t_{31}=t_{23}=t_{32}=1$, (14) is satisfied and we get

$$s=\frac{1}{1-\alpha} \quad m=\frac{\alpha}{1-\alpha}. \tag{15}$$

The corresponding structure is shown in Fig. 5. The other one-multiplier structures in [3] can similarly be obtained by appropriate choices of $\boldsymbol{T}=[t_{ij}]$.

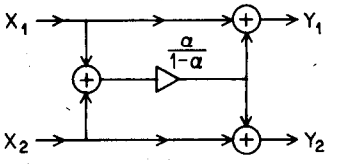

Fig. 5. One-multiplier realization for the LPC lattice.

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An Efficient Technique to Improve NORA CMOS Testing

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Abstract — **This paper presents a novel circuit technique to improve the testability of NORA (NO RAce) CMOS circuits. It is based on the structure, properties and operations of NORA CMOS. The precharge and evaluation properties of NORA CMOS enable one to design simple testing circuit for output stuck-at-zero, stuck-at-one, stuck-open and stuck-on faults. Area and time considerations, as well as the applications of this testability enhancement technique are also discussed.**

I. Introduction

With the increase in the complexity of VLSI systems, testing has become more difficult and this has been the motivation for adopting "design for testability" strategy in which several design techniques are used to make testing manageable and economical. An example of such methods is the built-in-self-test (BIST) technique, which has been introduced to achieve more economical and effective testing strategy [6]. In this approach, the implementation technology has a great impact on the testing technique to be used which has necessitated developing special methods for each technology. Testing NORA (NO RAce) CMOS [1], [2] is the main scope of this paper.

NORA is a racefree dynamic CMOS for pipelined logic structures [2]. It operates using two clocks in racefree fashion regardless of their overlap time and clock skew. The importance of NORA circuits stems from this property which overcome several problems of Domino CMOS circuits [2].

The main building block of NORA technique is shown in Fig. 1. Two clocks ϕ and $\bar{\phi}$ are provided. During the precharge phase

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